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INVESTIGATION ON THERMAL PERFORMANCE OF PRIMARY AND SECONDARY THERMOELECTRIC MODULES

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ABSTRACT

This paper reports the findings of an investigation on application of secondary thermoelectric (TE) module as a heat exchanger for the primary TE module. The experimental system consists of two commercially available thermoelectric modules arranged thermally in series with a heat sink and an integrated circuit (IC) chip. Heat produced from the IC chip is transferred to the heat sink via the TE modules. A total of nine experimental setups were analyzed using measured temperature data to assess the efficacy of the setups.

Experimental evidence shows that the secondary TE module provides additional cooling advantage. The cooling capacity for a system with secondary TE module is 10.95W compared to 3.5W for systems where secondary modules are non-existent. The respective coefficient of performance, $COP = Q_c / Q_p$ are 2.43 and 0.78. The use of a secondary TE module as a heat exchanger for the primary thermoelectric module is ineffective when compared with liquid-cooled heat exchanger.

Results further showed that during early stages of heating and cooling processes, there exists lag in response time between the integrated circuits chip. This could result in over-heating or under-cooling the IC chip.

Keywords: Thermoelectric, primary, secondary, heat exchanger, integrated circuit chip, heat transfer, experiments, and coefficient of performance.

INTRODUCTION

The maximum power dissipation of a single chip package is predicted to be 170W in 2008, [1], while maintaining the maximum junction temperature at 85°C or less. According to Intel's predictions, within the next five to ten years, the increasing power requirements of the IC chip is going to exceed the cooling capability of current techniques, Zhang et al. [2]. As a rule of thumb, a 10°C rise in temperature is equivalent to a factor-of-two increase in observed failure rate, Hannemann et al. [3]. The current trend in electronics is that the expected speed of processors doubles every two years. This is mainly achieved by reducing the path of the electric signal, thus increasing the speed.

Pool boiling, detachable heat sinks, channel flow boiling, micro-channel and mini-channel heat sinks, jet-impingement, and sprays are capable of dissipating over 100 W/cm^2 using dielectric coolants known to possess relatively poor thermal transport properties, Muduwar [4]. Miniature refrigeration systems have been designed for a heat load of 350W and operating temperatures of 12°C, Chein et al. [5]. Even though passive cooling systems can handle high heat loads, maintaining the junction temperatures at 85°C or even lower is a challenge due to working fluid limitations. Also miniature refrigeration systems have not been made commercially available, Chein et al. [5]. In light of the limitations in the heat removal capability of forced air and other fluid based cooling systems, the need arises for consideration of solid-state based device such as thermoelectric, TE, for

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cooling of electronics. The advantages of using TE cooling includes high reliability, flexibility in packaging, lesser weight and maintaining lower junction temperatures.

Thermoelectric cooling uses solid state devise based on Seebeck, Peltier, Joule, and Fourier effects to pump heat away from a heat source, with no moving parts or fluid movement. Thermoelectric are manufactured in modular form, where a series of p-type and n-type semiconductor element junctions are sandwiched between ceramic plates. The ceramic plates are used to restrict the flow of electrical current into the device that is being cooled, but allows heat to pass through easily. At the cold junction, heat is absorbed by the electrons as they pass from a low energy level in the p-type element to a high energy level in the n-type element. The passage of current causes electrons in the n-type material to move toward the hot end, and holes in the p-type material also move toward the cold end. Both the electrons and holes carry thermal energy. So, the result is a net flow of heat from the cold end to the hot end, where the heat is rejected. The principles of the various effects can be obtained from [6-10].

Typically, the TEM is sandwiched between a heat source and a heat sink, with the cold side of the TEM attached to the heat source. The heat sink could be an air or liquid system. A combination of TEM and the active heat sink offers far more cooling capacity than a heat sink however the additional heat dissipation components increases the size of the overall cooling system. Simmon et al. [11], and Phelan et al. [12], in their work, demonstrated the applicability of TEM for electronics cooling however the design on the heat sink at the TEM hot side was not addressed in detail, [5]. Chein et al. [5], in their numerical work on thermoelectric cooler applications in electronic cooling, showed attaching microchannel heat sink on the hot side of TEM and using water as the working fluid results in lower thermal resistance. Nnanna et al [13] in their work on assessment of thermoelectric module using nanofluid heat exchanger showed that a lag-time exist between the thermal response of the TEM and heat exchanger; and that the lag is attributed to thermal contact resistance between the TEM and heat exchanger.

This paper examines the impact of various incarnations of thermoelectric modules, heat sink, and fan as a cooling system for integrated circuit chip. It compares a single- and two-TEM system with heat sink and fan assembly. The temporal evolutions of temperature on the cold-side, hot-side, heat source and heat sink were measured experimentally to study the cooling effectiveness of the TEM system.

NOMENCLATURE

COP	coefficient of performance
G	area / length of T.E. Element, *m*
I	current, Amps
IC	integrated circuit chip
κ	thermal Conductivity, *W/mK*
k	device thermal conductance, *W/ K*
N	number of TE elements
Q_c	TE cooling capacity, *W*
Q_p	power input to TE module, *W*
R	device electrical resistance, Ω
T_{ave}	$1/2\ (T_H + T_C)$, *K*
T_C	cold side temperature, *K*
TE	thermoelectric
TEM	thermoelectric module
T_H	hot-side temperature, *K*
ΔT	$T_H - T_C$, *K*
S	device Seebeck voltage, $2\alpha N$, *V/K*
Z	Figure of merit, $\alpha^2 / \rho\kappa$, *1/K*

Greek symbols

α	Seebeck Coefficient, *V/K*
ρ	Resistivity, Ωm

Subscripts

c	cold-side
h	hot-side

EXPERIMETAL APPARATUS

The schematic of the experimental facility is depicted in Fig. 1. It consists of TEM, an integrated circuit chip (heat source), heat sink and fan, temperature sensors, power supplies, insulation, and data acquisition system. The TE module is a commercially available Melcor's product, CP2-127-06l. The semiconductor of the TE module is Bismuth Telluride, Bi_2Te_3; its properties are provided in Table 1. The current input to the TE module is regulated using a 0-12Amp, 0-18V Scott Engineering power supply.

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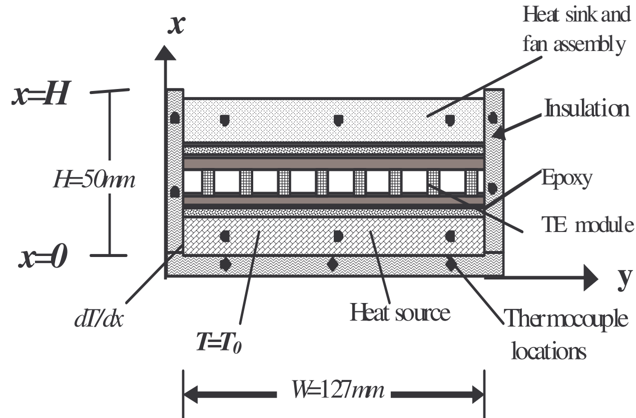

Figure 1. Schematic of the test apparatus

Table 1. Characteristics of TEM

Notation	Value	Unit
α, Seeback Coefficient	2×10^{-4}	V/K
ρ, Resistivity	1×10^{-5}	Ω .m
k, Thermal conductivity	1.50	W/m.C
A, Area of each semiconductor	1.17×10^{-5}	m^2
L, Length of each Semiconductor	4.49×10^{-3}	m
N, Number of Semiconductors	127	
R, Resistance	2.53	Ω

The heat source is a 2.5cm × 2.5cm foot-print area aluminum block with three through-holes drilled along its length for placement of heater cartridges. A total of three cartridges were used. Each generates a maximum of 150 Watts resulting in a maximum heat output of 450 W. The cartridges are electrically connected in parallel to each other to maintain a constant voltage across the heaters and also to increase power output. All the cartridges are connected to a HP6674A power supply which controls the voltage and current output from the heater.

The heat source is attached to the TE module using thermal conductive epoxy, OMEGABOND 201, to minimize thermal contact resistance between the module, heat source, and the heat sink. The thermal conductivity of the epoxy is 7.62W/mC

The "dark circles" shown in Figure 1 signify the locations where thermocouples are attached. The thermocouple is a copper- constantan, 40-gage T-type. Ten thermocouples attached to the IC monitors change in temperature; five arrays of three thermocouples, each array attached to the cold- and hot-side of the TEM, and with the other three arrays attached each to the bottom, base, and tip of the heat sink measure heat flow across the heat sink. Additional thermocouple locations not shown in Fig. 1, are used to estimate lateral heat loss through insulation, measure ambient temperature, and to use them as back up sensors in case of material failure.

All of the thermocouple wires were connected to two twenty-channel Reed plug-in module with a built-in temperature compensation for direct temperature measurement. Each module has twenty channels and communicates with the floating logic via the internal isolated digital bus of the data logger HP34970A. Temperature measurements from the data logger are automatically recorded in the personal computer for further data reduction. The error in the thermocouple readings is estimated to be ±0.2°*C* and verified under constant temperature condition.

As shown in Fig. 1, all the external surfaces of the test apparatus, with the exception of the heat sink were insulated with a 21.3*mm*-thick Polystyrene board in order to reduce heat losses from the sides to the surroundings. The thermal conductivity of Polystyrene board is ~0.027W/mK.

EXPERIMENTAL PROCEDURE

Figure 2 presents various setups that were fabricated for testing in this study. The setup in Figs. 2a-b has one- and two-TEMs respectively. Figures 2 c-e shows setups with heat sink, a single TEM plus heat sink, and two TEM plus a heat sink system, respectively. Figures 2(f-i) shows setups where a cooling fan was applied in addition to the TE module and heat sink. For setups where TE modules are applicable, the TEMs is sandwiched between the IC and heat sink using epoxy. The IC chip and TEM is connected to a 60V-35A HP6674A power supply and an 18V power supply, respectively. The fan is regulated using a PC power supply.

As a preamble to testing each experimental setup, the data acquisition system is activated and parameters such as the sampling rate, test period, gain, offset, etc, are programmed using BenchLink software. The sampling rate is 10s for each thermocouple location and the test duration is 6000s. Preliminary measurement of temperature is made with the heat source in off-position to ensure uniformity of initial temperature readings. These temperature data are benchmarked with measurements obtained from mercury-in-glass thermometer to verify accuracy in the thermocouple readings.

The experiment begins by initializing the scan command in the data acquisition system and simultaneously switching on the power supply that regulates the IC, TEM, and fan. Power produced from the IC module is absorbed by the cold-side of

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the TEM to the hot-side via the Bismuth Telluride semiconductor elements of the TE module. The hot-side of the TE thermally communicates with the heat sink as in Figs. 1 and 2. Temperature measurements were automatically recorded in a personal computer for further analysis.

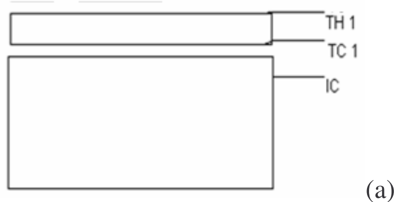
Several set of experiments were carried for each setup in Figs. 2 (a-i). A set of experiment consists of three tests performed at the same conditions to ascertain reproducibility of the temperature data. Table 2 provides a test matrix for some of the setups. It should be noted in Table 2 that for some cases, the IC power was deliberately switched-off, 0W, to study the thermoelectric module thermal response in the absence of a heat source.

Table 2. Test Matrix

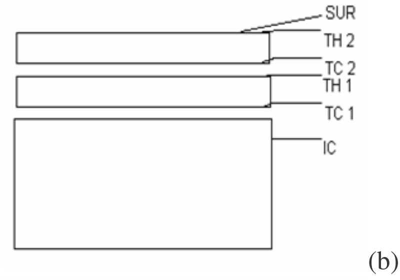
Cases	No. of Heat Sinks	No. of TEMs	Fan Power, W	TEM Power, W	ICchip Power, W
Fig. 2b	0	2	0	1	0
Fig. 2b	0	2	0	4.5	0
Fig. 2e	1	2	0	1	0
Fig. 2e	1	2	0	4.5	0
Fig. 2i	1	2	0.8	1	0
Fig. 2i	1	2	0.8	4.5	0
Fig. 2i	1	2	0.8	4.5	0.75
Fig. 2i	1	2	0.8	4.5	3.26
Fig. 2h	1	1	0.8	4.5	3.26
Fig. 2h	1	1	0.8	4.5	6.94

The main source of uncertainties is error due to the measurement of temperature, heat transfer rate, and physical dimensions. The combined uncertainty of the data logger HP34970A and the thermocouple calibration in the measurement of temperature is ±0.4% or ±0.5°C, whichever is greater. The error associated with heat transfer rate is due to voltage and current measurements, and are respectively, (U_v = 0.05% of setting + 90mV) and (U_I = 0.1% of settling +35mA). The combined uncertainty of the current and voltage in the heat transfer rate is expressed as

$$U_q = \sqrt{(U_I \partial q/\partial I)^2 + (U_V \partial q/\partial V)^2} \qquad (3)$$



(a)



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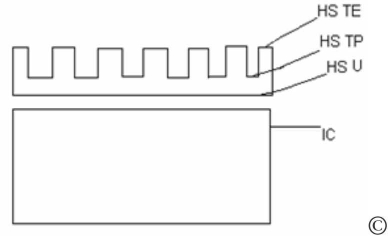

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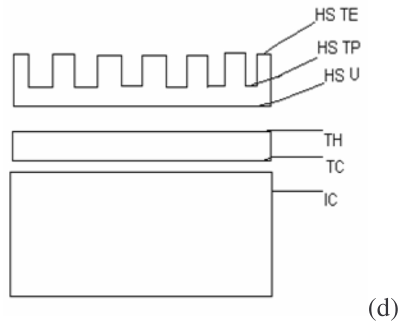

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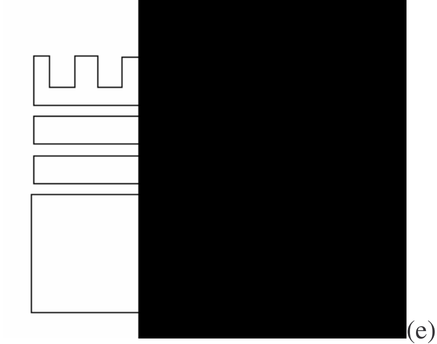
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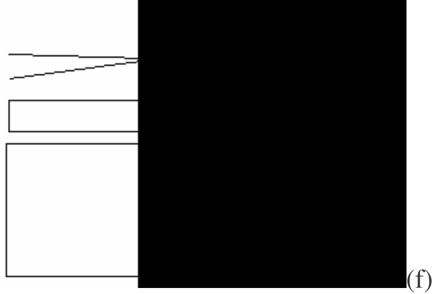
(f)

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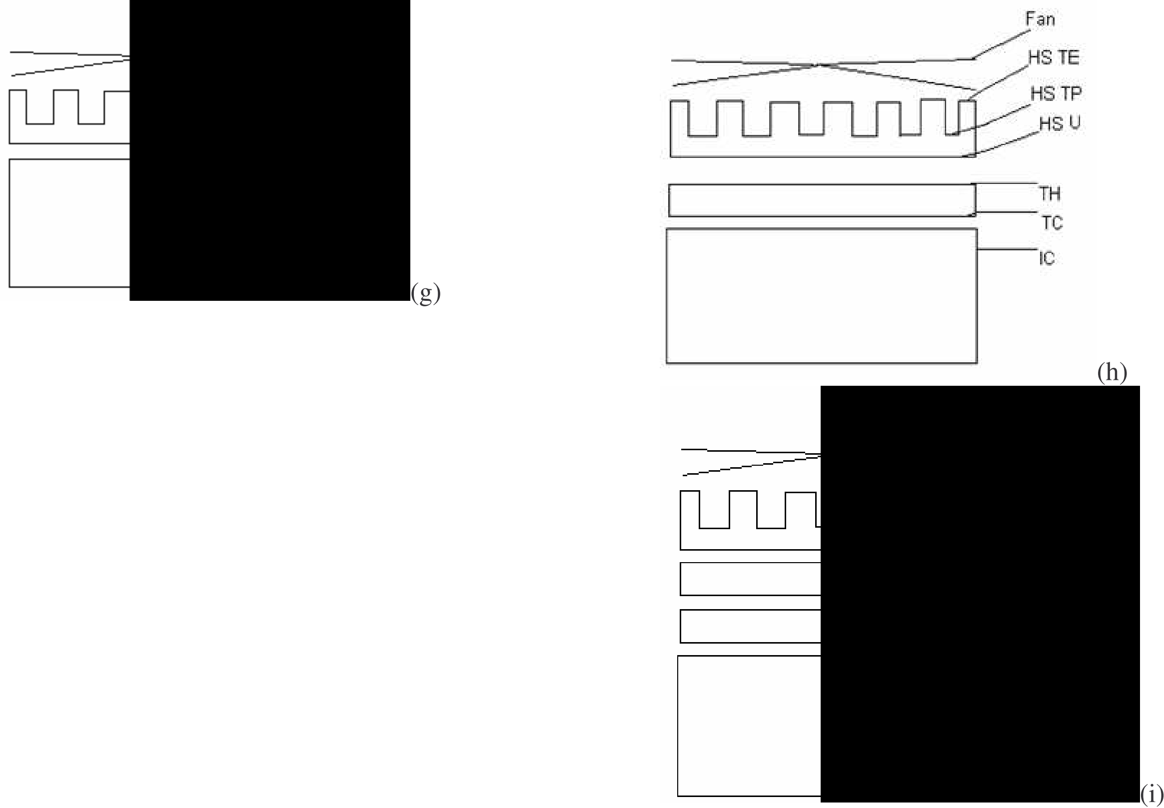

Figure 2. Test setup for various case studies. (a) one TEM, (b) two TEM, (c) heat sink with no TEM, (d) heat sink and one TEM, (e) heat sink and two TEM, (f) one TEM and fan, (g) heat sink and fan, (h) one TEM, heat sink and fan, and (i) two TEM, heat sink and fan.

RESULTS AND DISCUSSIONS

The heat transfer performance for experimental setups shown in Figs. 2a, 2c, 2d, 2f, and 2g are poor, they maintained the junction temperature at a much higher value in contrast to setups in Figs. 2b, 2e, 2h, and 2i. Hence, for brevity, only sample of measured temperature data for Figs. 2b, 2e, 2h, and 2i will be reported herein. Table 3 presents the average steady-state temperature data for Figs. 2b, 2e, 2h, and 2i. An assessment of data in Table 3 reveals that under the same heat load conditions, the thermal performance of Fig. 2i (two TEMs, heat sink and fan) is better than Fig. 2h (one TEM, heat sink and fan). For a heat load of Fig. 2i and 2h maintained the IC chip temperature at 39.1˚C and 40.5˚C, respectively; which is about 3.6% difference. The corresponding temperature difference, ΔT, between the hot- and cold-sides of the primary thermoelectric modules in Figs. 2i and 2h are 16.3˚C and 24˚C, respectively.

Table 3. Heat transfer data for some setups in Figs. 2

Cases	No. of Heat Sinks	No. of TEMs	Power Fan, W	Power input TEM, W	Power IC, W	TC1, C	TH1, C	ΔT1, C	TC2, C	TH2, C	ΔT2, C
Fig. 2b	0	2	0	4.5	0	37.6	52.9	15.3	55.8	72.1	16.3
Fig. 2e	1	2	0	4.5	0	31.9	47.7	15.8	45.6	64.2	18.6
Fig. 2h	1	1	0.8	4.5	3.26	43	67	24	0	0	0
Fig. 2h	1	1	0.8	4.5	6.94	50	73	23	0	0	0
Fig. 2i	1	2	0.8	4.5	0	19	29.9	10.9	30	47.4	17.4
Fig. 2i	1	2	0.8	4.5	0.75	27.8	39.2	11.4	39.9	56.8	16.9
Fig. 2i	1	2	0.8	4.5	3.26	40.8	57.1	16.3	57.9	72.1	14.2

This difference in performance is due to the secondary thermoelectric module present in Fig. 2i setup. The secondary module served as a heat exchanger to primary TE module that is in direct contact with the IC chip. Hence, the thermal enhancement of Fig. 2i is attributed to the cooling effect caused by the secondary TE module.

The use of a secondary TE module as a heat exchanger for the primary thermoelectric module is ineffective when compared with liquid-cooled heat exchanger as reported in Nnanna et al. [13]. In their experimental work on assessment of the thermoelectric module (Melcor's product, CP2-127-06l) using nanofluid heat exchanger, they reported that for maximum IC chip power of 78.5W, the junction temperature was maintained at 54˚C; whereas when a secondary TE module is used as a heat exchanger, for a maximum chip power of 3.27W, the chip temperature is 39.1˚C.

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The thermal resistance across components such as the IC chip and thermoelectric module can be estimated based on energy balance. The thermal circuit diagram for Figs. 2i and 2h are shown respectively in Figs. 3a and 3b; Q_c, Q_H, and Q_p refers to TE module cooling capacity, heat transferred from the hot-side of the TE module and power input to the TE module, respectively.

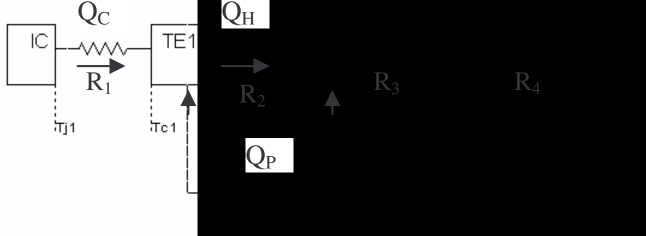

Figure 3a. Thermal circuit diagram for Fig. 2i

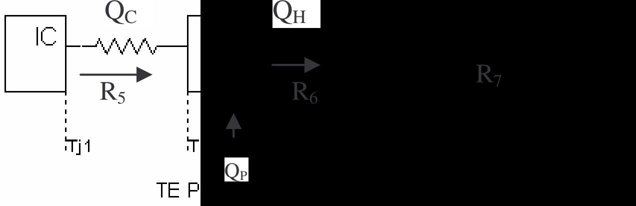

Figure 3b. Thermal circuit diagram for Fig. 2h

The thermal resistance is expressed as $R=\Delta T_R/Q$. That is, $R_1 = (T_{j1} - T_{c1})/Q_c$, where $Q_c = \alpha I T_c - .5 I^2 R - k\Delta T$. Note that $\Delta T_R \neq \Delta T$; $\Delta T = T_h - T_c$ is the temperature difference between the hot- and cold-side of the TE module whereas ΔT_R refers to temperature difference between any two components. The subscript "R" represents resistance. Based on data in Tables 1 and 2, The Q_C for Figs. 2h and 2i are respectively 3.5W and 10.95W for Q_p of 4.5W. The respective coefficient of performance, $COP = Q_c/Q_p$ are 0.78 and 2.43.

Figure 3 presents the temperature profiles of experimental setups Fig. 2i and 2h. It shows the temporal evolution of the heat source temperature, Ts, and the hot- and cold-side temperature for the primary TE modules. According to data in Fig. 3, $(\Delta T_{Fig.2h}) > (\Delta T_{Fig.2i})$, where $\Delta T = T_h - T_c$ is the difference between the hot- and cold-side temperature of the TEM. To better understand the physical meaning of $(\Delta T_{Fig.2h}) > (\Delta T_{Fig.2i})$, we examine the definition of TE module coefficient of performance (COP). The COP is expressed as $COP = \frac{\alpha I T_c - .5 I^2 R - k\Delta T}{I(\alpha \Delta T + IR)}$, where $\alpha I T_c$ is the Peltier effect, $0.5 I^2 R$ is the Joule heating effect, and $k\Delta T$ is the Fourier effect. The numerator and denominator of the COP equation represent the cooling capacity and power input to the TE module, respectively. An inspection of the COP equation reveals that increase in Fourier effect decreases the coefficient of performance by decreasing the cooling capacity and increasing the TE module power requirement. Assuming that the thermal conductivity, k, is constant, an increase in Fourier effect is caused by ΔT. Therefore, $(\Delta T_{Fig.2h}) > (\Delta T_{Fig.2i})$ signifies that the Fourier effect is more pronounced for the setup in Fig. 2h than Fig. 2i. With the ($T_{c, Fig. 2h}$) < ($T_{c, Fig. 2i}$) as shown in Table 1, and $(\Delta T_{Fig.2h}) > (\Delta T_{Fig.2i})$; the coefficient of performance of the setup in Fig. 2i is higher that of Fig. 2h.

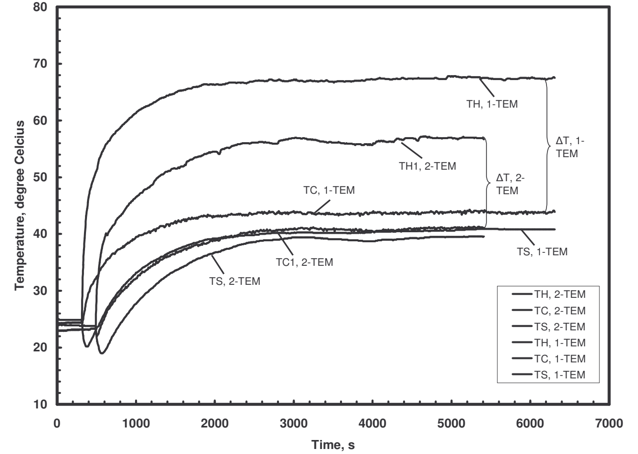

Figure 4. Temporal evolution of temperature for Figs. 2h and 2i

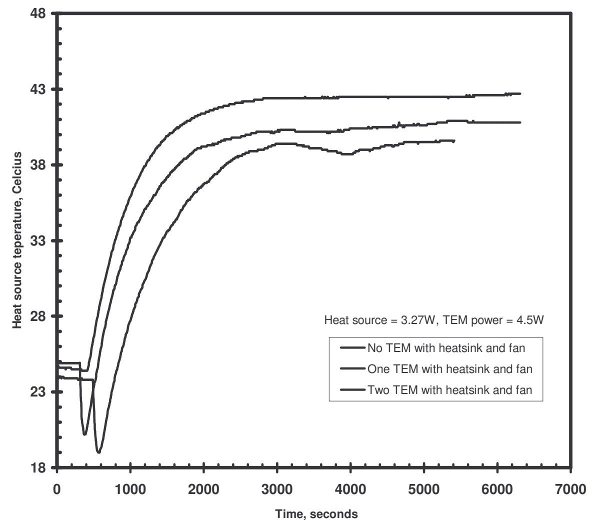

Figure 5. Variation of the heat source temperature with time

It is observed in both Figs. 4 and 5 that during early stage, $0 \le t \le 80s$, of the heating process, the heat source (IC chip) temperature decreased by 5 °C, approximately at the cooling rate of 0.059°C/s, whereas the TE module cold- and hot-side temperature increased during the same time frame. The heat source temperature began to increase when $t > 80\sec$ as illustrated in Fig. 6. This behavior is attributed to the difference in the response time between the heat source and the thermoelectric module. The heat source may have a long response time hence requires longer time to cause an appreciable temperature change whereas the TE module has a short response time.

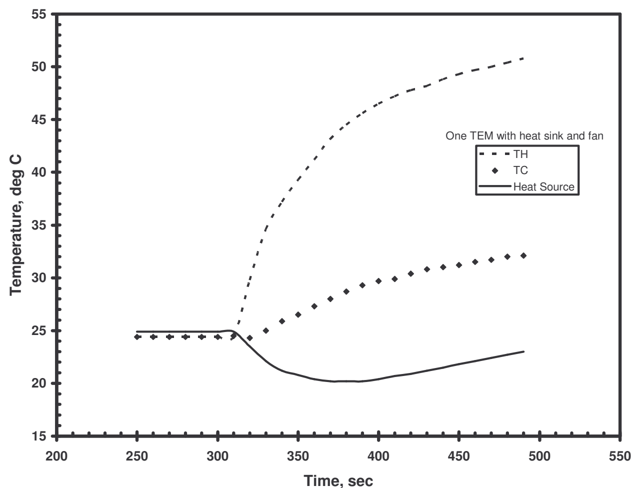

Figure 6. Temperature profiles during early stage of heating process

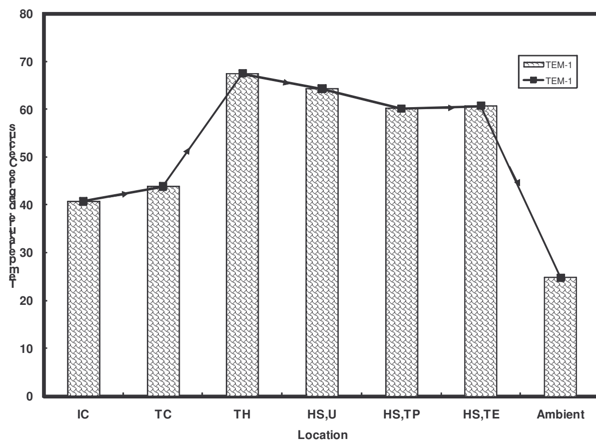

Figure 7. Spatial evolution of temperature

Figure 7 presents the average steady-state temperature at prescribed locations in the direction of heat flow. These locations are at the IC chip, cold- and hot-side of TE module; bottom surface, base, and tip of the heat sink, and the ambient. Each data point represents average steady-state temperature measurement at these locations. As expected, the temperature profile reveals that heat is transferred from the cold-side to the hot-side of the TEM, and from the hot-side to the ambient. The temperature gradient between the cold- and hot-side (T_C and T_H) is indicative of the thermal resistance, $R = \Delta T / Q$ associated with the TEM P-type and N-type semiconductor, and the ceramic substrates.

CONCLUSIONS

Experiments to study the use of secondary TE module as a heat exchanger have been performed. This is significant and has potential application for cooling microelectronics device particularly when space is limited for installing active cooling system. The experimental apparatus consists of two commercially available thermoelectric modules arranged thermally in series with a heat sink and an integrated circuit (IC) chip. Heat produced from the IC chip is transferred to the heat sink via the TE modules. A total of nine experimental setups were analyzed using measured temperature data to assess the efficacy of the setups.

Experimental evidence shows that the secondary TE module provides additional cooling advantage. The cooling capacity for a system with secondary TE module is 10.95W compared to 3.5W for systems where secondary modules are non-existent. The respective coefficient of performance, $COP = Q_c / Q_p$ are 2.43 and 0.78. The use of a secondary TE module as a heat exchanger for the primary thermoelectric module is ineffective when compared with liquid-cooled heat exchanger.

Results further showed that during early stages of heating and cooling processes, there exists lag in response time between the integrated circuits chip. This could result in over-heating or under-cooling the IC chip.

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